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RESEARCH ARTICLE

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DEVELOPMENT OF TRANSISTORIZED INVERTER SYSTEM USING NANOTECHNOLOGY AND ITS CHALLENGES

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ABSTRACT

This paper presents the development of transistorized inverter system using Nano-technology and its challenges. An inverter is used for conversion of direct current (d.c) to alternating current (a.c). The research is mainly on transistor switch type inverter using Nanoscaling system, aiming to cope with variations, power saving and to track an optimal energy operational point notwithstanding challenges. In testing, the equipment, its was observed that as the input supply increases, the two lamps were brighter until a maximum of 6 volts was attained at the input. The testing and measurement arrangement was done by connecting multi-meter probe through the output terminal of the step-down transformer to know the output voltage. It was recorded that, the higher the input voltage, the higher the output. With these, a robust portable transistorized inverter system can be developed.

 T_{ox} – Oxide thickness, V_{th} – Threshold voltage, Nm – Nanometer, C_{ox} – Oxide capacitance, I_d – Drain current, V_{GS} – Gate-source voltage, V_{DS} _– Drain-source voltage, and E_{ox} – Electric field oxide

Introduction

As a result of basic research on the physics of solids, transistors had paved ways for a new generation of powerful and efficient electronics devices (inverter) with seemingly unlimited numbers of application in everyday life. As a consequence of the continuous improvement in technologies, transistor can be fabricated using Nano-scale technology.

The economic importance of this system is to cope with variations, save power consumption. In literature, so many inverters system has been developed but with variation's challenges. Moore predicted in 1998 an exponential relationship between device complexity (no. of transistors per area unit) and time, by stating that 'the complexity will double – annually'. This prediction has in mean time revised to a doubling every two years [6,13], resulting in over 5 billion transistors being processed on a single chip today. As a consequence of complexities, transistors have to be down scaled to the deca – nano – meter regime (Nanotronic) which has resulted in a reliable devices development architecture devoid of complexity.

This paper will describe development of transistor switch – type inverter using nano–scaling and challenges in fabricating the transistor.

Materials and Method

The major components of the circuits are;

- ransistors: these are used in the circuit to control the flow of current through load
- Resistors: these are for the biasing of the transistors. The rating is such that, the voltage drops across them are suitable for the proper operation of the transistors
- ➤ Capacitors: they performed the function of coupling signals from one transistor to the other, as such coupling capacitors can be used.
- ➤ Transformer: the power transformer used in this circuit is the step up type, it therefore helps in stepping up the already amplified output signal and further couples it to the output

Transistor's fabrication/ scaling trend

While decades ago, transistor structures were processed in the micrometer range, modern transistors structures have been scaled down to 22nm in 2008 and to 14nm in the current generation of transistors. In addition to the scaling of the width (w) and length (L) of the transistors, the thickness (t_{ox}) has also been scaled down reaching values less than 2nm. Considering SiO₂ as the insulating material, 2nm in fact contain a rather small number of layers of atoms as shown in fig 1.

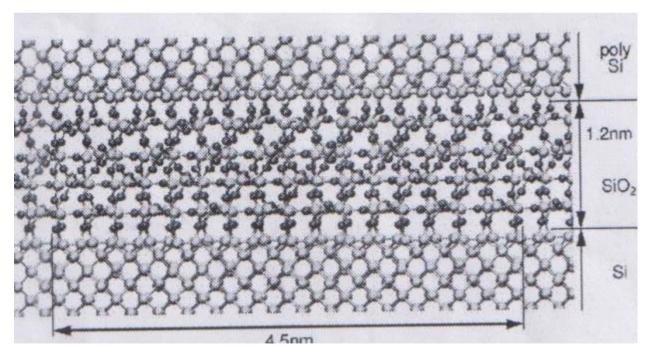


Fig.1 Schematic atomic structure of the nanoscale transistor (source: *Ulmann B & Grasser T. (2017) transformation: nanotechnology – challenges in transistors design*)

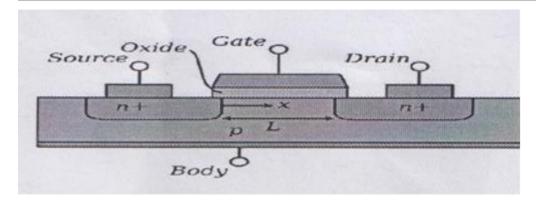


Fig.2 Two n-doped source and drain region separated by a p-doped body region (source: *Ulmann & Grasser* (2017) 'transformation: nanotechnology – challenges in transistors design)

On top of this a 14nm thick Au layer was deposited as source and drain electrodes. The dielectric layer was applied over the semi – conductor by spin coating, on top of the dielectric, the electrode was deposited. The insulating layer is sandwiched between the gate and the body (substrate) separating them from each other and thus preventing a current flow, (Fig1 and 2). The scaling results in several designs and fabrications

Scaling / fabrication challenges

The scaling of the geometry results in several design and fabrication challenges, for example a short transistor length (less than 100nm), leads to channel effect example drain – induced barrier lowering, which affects the transistor performance [6].

Additionally, channel leakage currents are more pronounced, therefore, the off – current increases significantly. Moreover, considering that;

$$C_{ox} \alpha A/t_{ox}$$

Where $A = L \times W$ is the area, t_{ox} has to be scaled in the same manner as A. otherwise, C_{ox} would increase significantly which would have a great impact on V_{th} (threshold voltage) and the switching dynamics. However, t_{ox} is limited to a certain minimum value because of quantum effect like tunneling leading to a dramatic increase of leakage currents if the oxide thickness is further reduced. With a t_{ox} below this value, a loss–less control cannot be ensured any longer. Furthermore, the supply voltages cannot be scaled in the same manner as the device geometry, otherwise, the ratio between the on and off current would deteriorate. Also, the electric field in the oxide E_{ox} has increased considerably due to indirect proportionality to t_{ox} . As a consequence, degradation effect depending on E_{ox} have a greater impact than in devices with thicker oxides [3,16].

Another consequence of down scaling is a higher variability due to the variance of parameters between transistors produced in the same manner. The variance is higher for nanoscale devices than for large devices in the micrometer range because nanoscale devices contain, in contrast to large devices only a countable number of discrete dopants. The slightest deviations of their number of positions influence the non – uniformly current flow over the width, the so-called percolation path. [2,7]

Circuit description

The inverter circuit uses the principles of transistor switch; hence the proper understanding of the circuit is necessary for a brief look at the switching principles of a transistor.

Transistor as a switch: one of the important applications of a transistor is to control the flow of current through a load in a manner similar to a switch. In practices, the transistor is operated based on the principle of triggered switch circuit. There are 3 basics types, classified according to the stability of their operating states;

- ➤ Bi stable: with two stable state between which it can operate
- ➤ Mono stable: with one semi stable and one stable state and returns to the stable state after a fixed delay period and
- ➤ The inverter circuit: the astable multivibrator which continuously oscillates back and forth between two semi-stable states providing a useful source of square wave which can be filtered to give sine wave.

In this case there is no stable state, but the circuit remains in quasi – stable state, with a particular transistor alternatively off and on for the periods determined by the time constants $R_1 C_1$ and $R_2 C_2$.

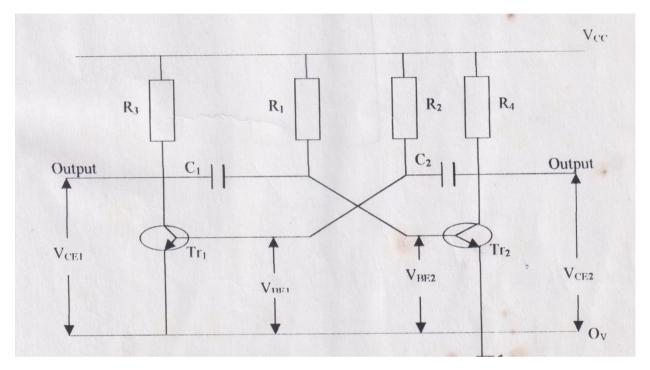


Fig.3 Astable multivibrator circuit

Device modelling

The drain current (I_D) of the transistor can be modelled with the variable range hopping model [15] as given by equation (1) and (2). In the below equations, V_{GS} , V_{DS} represent the gate – source and drain – source voltage of the transistor respectively. γ is a fitting parameter that accounts for the width of the density of state distribution of the semi – conductor and λ is the channel length modulation parameter.

Here the parameter β is given by

 $\mu C_{ox}/L$,

where μ , C_{ox} , W and L are mobility gate oxide capacitance, width and length of the transistors respectively

System operation/ working principle

An inverter is a device that changes d,c power into a.c power. The basic working principle of the system may be explained with the help of the circuits (fig.3 and 4). It is called voltage – driven

inverter because a d.c voltage source is connected through semi – conductor switches directly to the primary of a transformer.

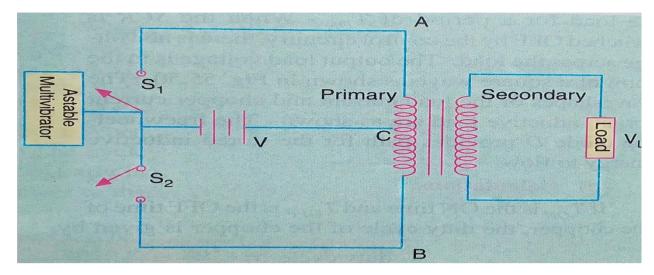
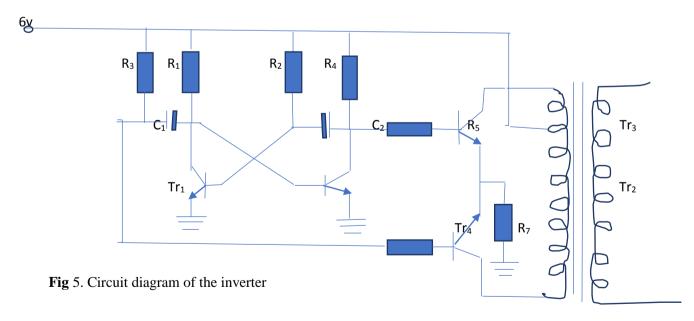


Fig.4 Picture diagram of a stable multi-vibrator (source: electrical technology textbook by Theraja, (1939))

 S_1 and S_2 are switching devices (transistors) which open and close alternatively at regular intervals of time. The two switching devices are generally driven by an astable multi – vibrator operating at the desired frequency. When S_1 is closed, the entire d.c source voltage V is applied across points A and C of the transformer primary. S_1 remains closed for a certain period of time after which it cut – off and S_2 closes. It also remains closed for the same period of time during which the source voltage V is impressed across points B and C of the primary. S_2 then opens out and S_1 closes. In this way an alternating voltage is applied across the primary which induces an a.c voltage on the secondary. Since d.c supply voltage is connected directly across the primary, the output waveform of the secondary voltage is a square wave. Irrespective of the type of load and load power factor, however the waveforms of both the primary and secondary currents depend on the type of load whether resistive, inductive or capacitive



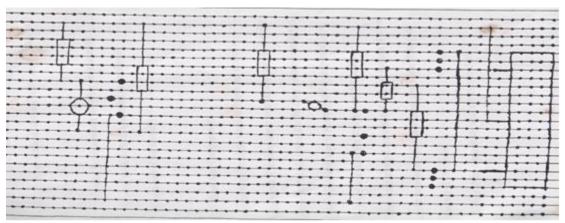


Fig 6. Layout circuit diagram of the inverter system

Circuit specification

The specification is not very rigid but varies between these extremes depending on the input voltage

	Maximum	Typical
Input voltage V_{in}	12Vdc	6Vdc
Output voltage V_{out}	240Vdc	120Vdc
Current output Iout	3.6mA	1.8mA
Power output Pout	0.86W	0.432W

Test and measurement

In testing, the equipment, it was observed that as the input supply increased, the two lamps were brighter until a maximum of 6Volts was attained at the input (fig. 7).

Voltage gain measurement

The testing and measurement arrangement (fig.7) is as shown; where meter was used to know the output a.c voltage that was connected through the output of the terminal of the step-up transformer.

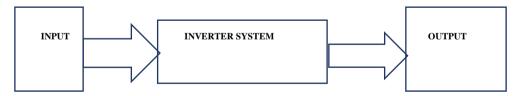


Fig.7: Diagrammatical testing/measurement arrangement of the system

It was recorded that the higher the input voltage, the higher the output. At 6V input, the output was observed as 20V. Therefore, voltage gain = 20/6 = 3.3Volts

Current measurement:

Input current = 0.172A

Output current = 0.023A

Voltage measurement:

Input voltage = 6V

Output across transformer = 20V

Efficiency of the system = output/input

Output power:

Root mean square (rms) value of the product of the max voltage swing and max current swing. That is

$$P = V_p \, x \, I_{max} / 6$$

 $= 20 \times 0.023/6 = 0.0767W$

Input power = V_{cc} x Average current

Therefore:

Power efficiency = $0.0767 \times 0.172 \times 6 / 0.636 = 0.12$ or 12%

Therefore, percentage power efficiency = 12%, displaying the waveform which is square, the waveforms appear better at lower input voltage supply and as the supply is increased, the distortions increase with it diminishing wave formed

Conclusion

We had analyzed the performance of the transistors with respect to their suitability for the design and construction of a transistorized inverter system using nanoscale. Though some challenges were faced, innovation approach have been suggested to overcome the challenges. All the same, from the calculated efficiency of the system, the performance was good.

Recommendation

Though the system was only experimental which with more research on it, would be developed to a rugged system that can drives some electrical appliances like electric motor etc. Recommended for more research on, so as to erode challenges in the cause of the system development.

REFERENCES

- [1] Amost, W (1971) 'Principles of transistor circuit', 5th edition. pp 17 30
- [2] Bina, M., Triebl, O., Schwarz, B., Karner, M., Kaczer, B., Grasser, T. (2012) 'Simulation of reliability on nanoscale devices'. In proc. of the international conference on simulation of semiconductor processes and device, SISPAD (pp. 109 112)
- [4] Ciocolette, J (1979) 'Electronic designer handbooks' pp 24 55
- [5] Cheong Hor, H.; Siek, L (2012) 'Review on VCO based ADC in modern deep submicron CMOS technology'. In: IEEE international symposium on radio frequency integration technology (RFIT); pp 86 88
- [6] Gelinck, H, Van-Veenendaal, E., Meijer, J., Cantatore, E., Edzer, H., Huitema, A. (2006) 'From transistors to large scale integrated circuits; Organic electronics materials, manufacturing and applications'. Weinheim: wiley VCH pp325 343

- [7] Gerrer, L., Hussin, R., Amoroso, S., Franco, J., Weckx, P., Simicic, N., Horiguchi, N., Kaczer, B., Grasser, T., Asenov, A. (2015) 'Experimental evidences and simulations of trap generation along a percolation path'. In Proc. of the 45th European solid state device research conference pp 226 229
- [8] Ghetti, A., Compagnoni, C. M., Spinelli, A.S., Visconti, A. (2009) 'Comprehensive analysis of random telegraph noise instability and its scaling in deca nanometer flash memories,' IEEE Trans. Electron devices 56 (8); pp 1746 1752
- [9] Harman, L. (1979) 'Fundamental of electronics textbook'; 2th edition of Lunch and Son's Inc.
- [10] John, W. (1948) 'Electronic engineers of the westling house'; industrial electronics reference book, Wiley and Son's Inc.
- [11] Moore, G.E., (1998) 'Cramming more components onto integrated circuits': Proc. IEEE, 86(1) pp 82-85
- [12] Retrieved 21 September 2017 from https://www.wikipedia.org/field-effect transistor
- [13] Retrieved 10 October 2019 from https://www.wikipedia.org/multigate device
- [14] Robertson, J. (2001) 'High dielectric constant oxides.' Eur. Phys. Appl. Phys. 28 pp 265 291
- [15] Theraja, L and Theraja, K (1939) 'Electrical technology textbook'; int edition, S. chand and co. ltd
- [16] Ullmann, B and Grasser, T. (2017) 'Transformation: nano-technology, challenges in transistor design and future technologies', *journal of electrotechnik and informationstechnik 134/7: pp* 349 354 Doi 10.1007/s00502-017-0534-y
- [17] Wilk, D., Wallace, M., Anthony, M. (2001) "High-k gate dielectrics: current status and materials properties considerations". *Journal of Appl. Phys.* 89, pp5243